

FIG. 1

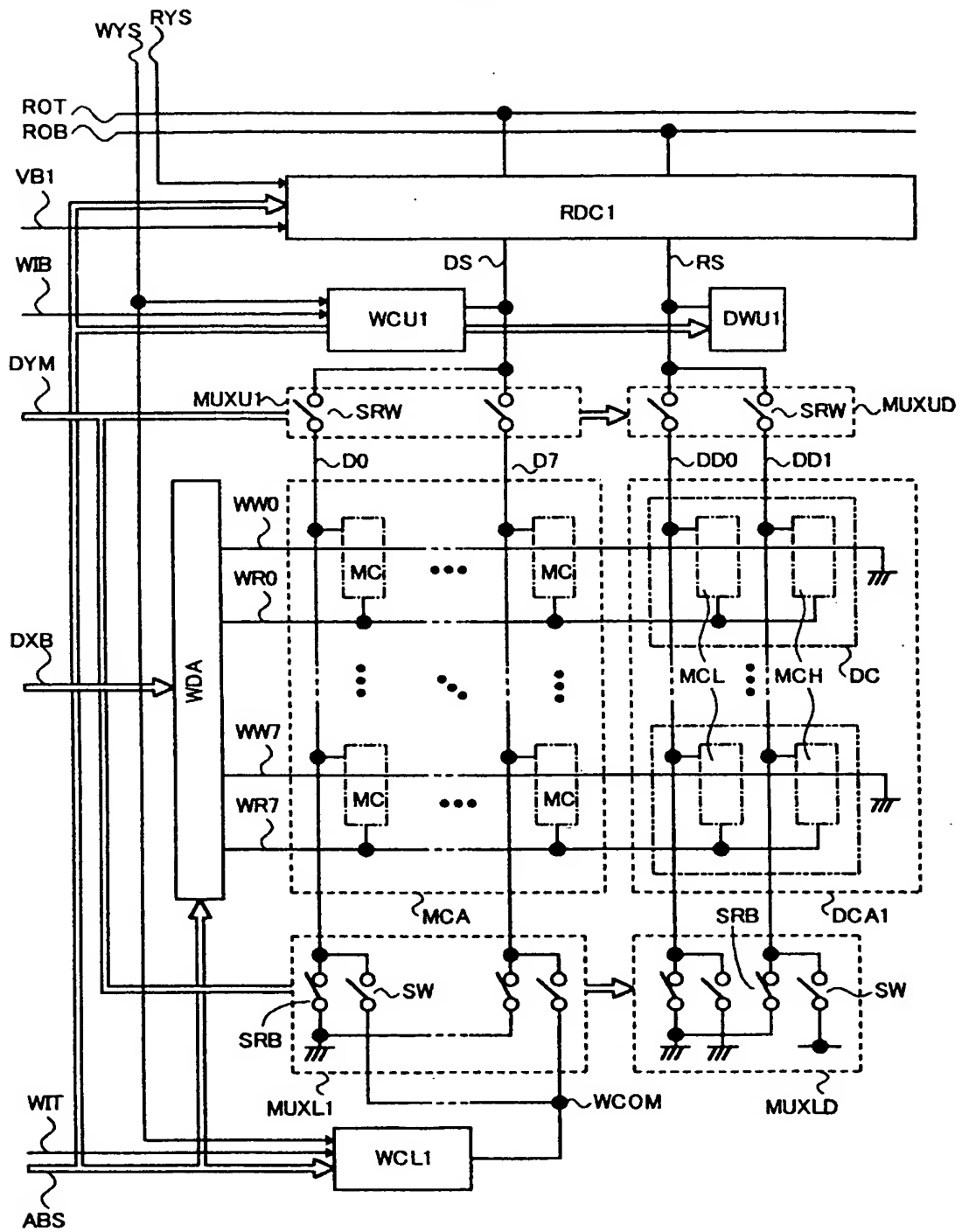


FIG. 2

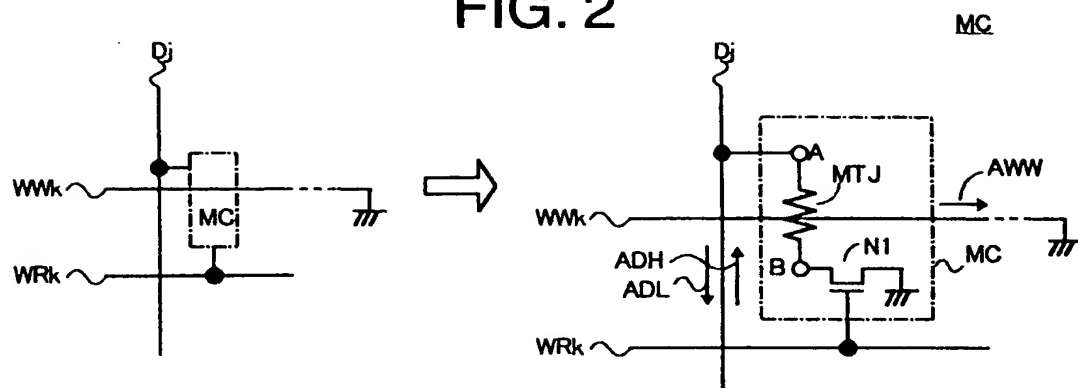


FIG. 3

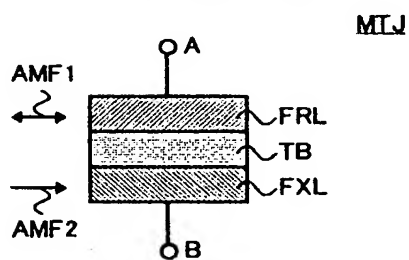


FIG. 4

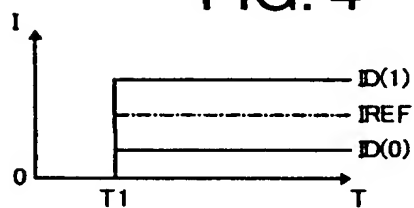


FIG. 7

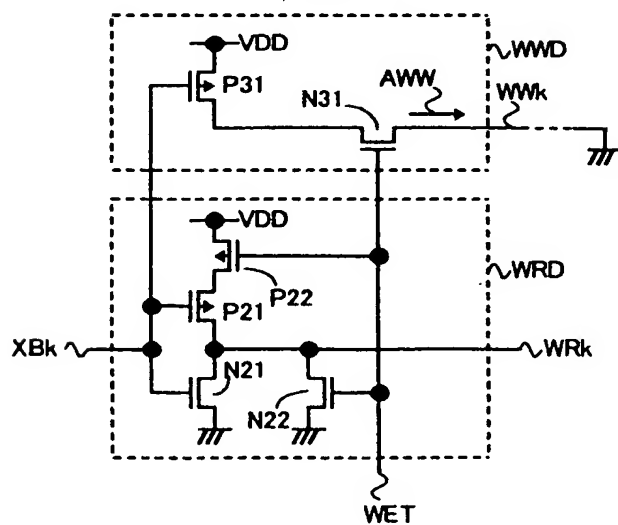


FIG. 5

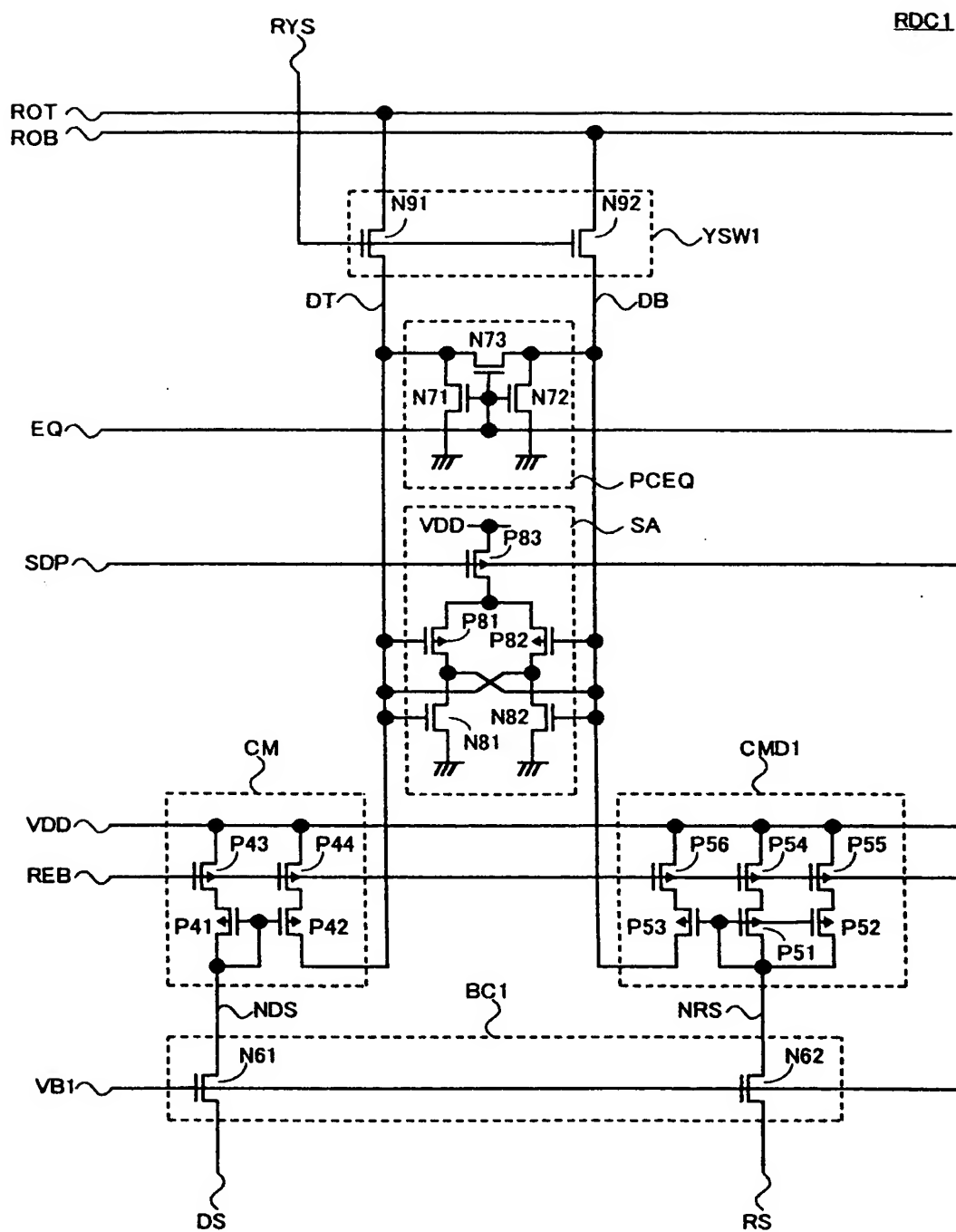


FIG. 6

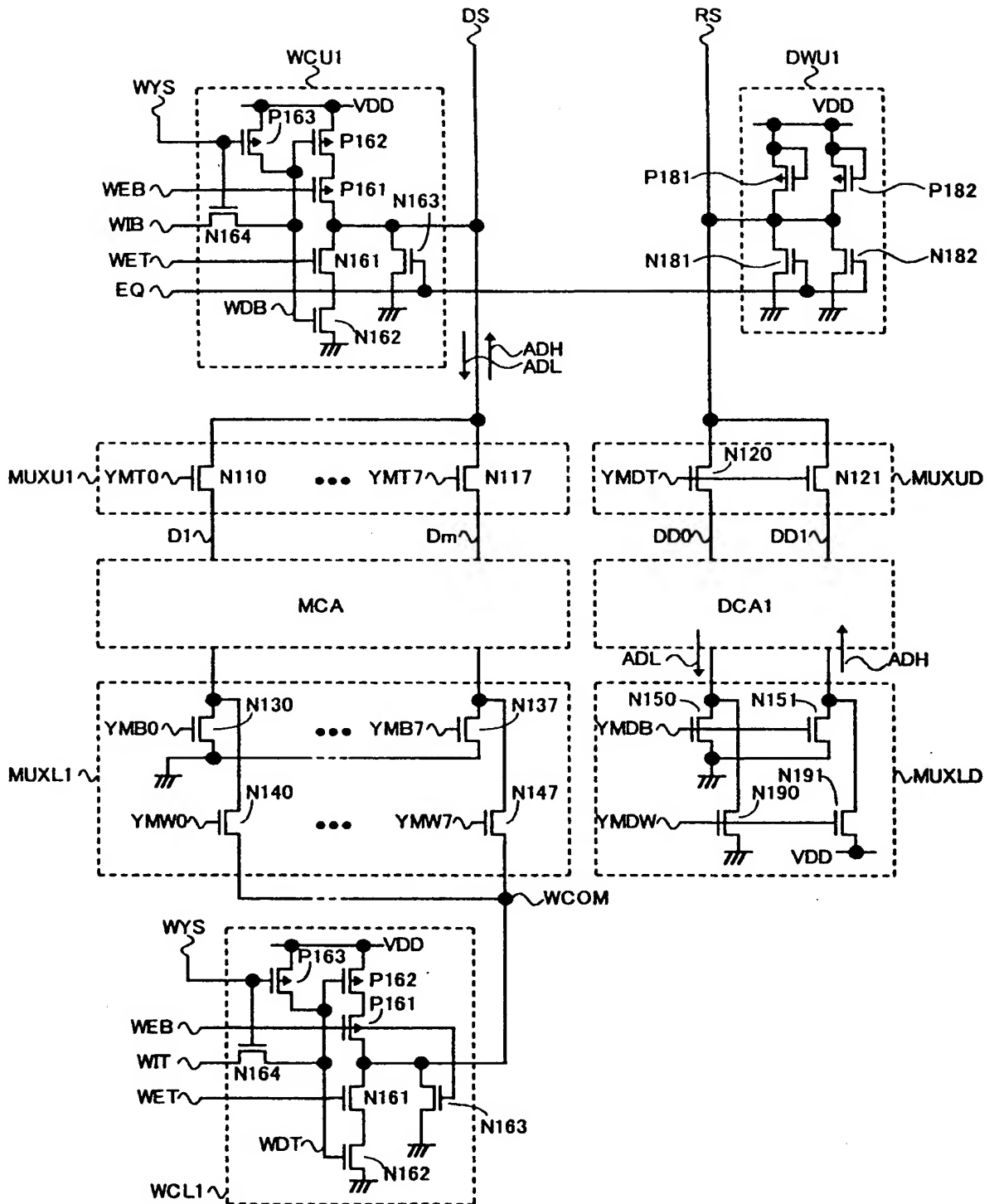


FIG. 8

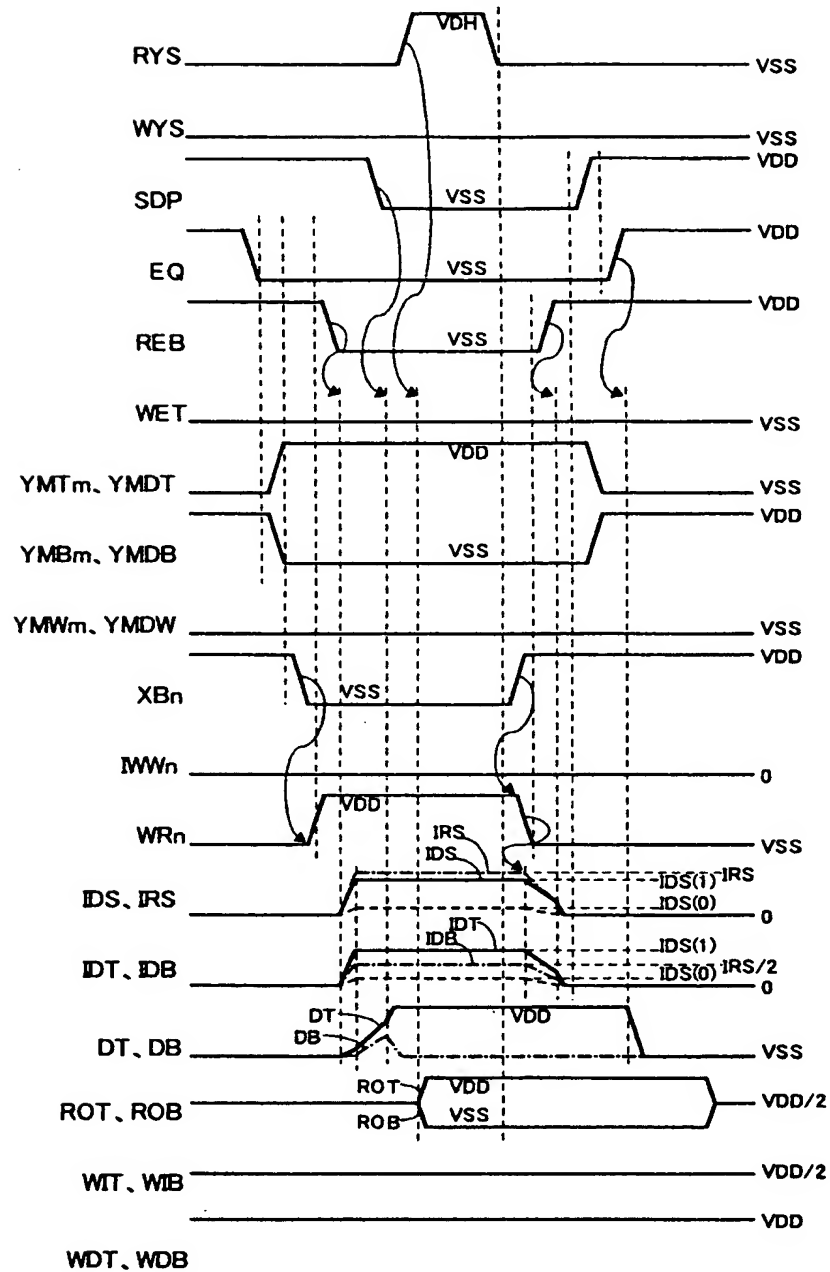


FIG. 9

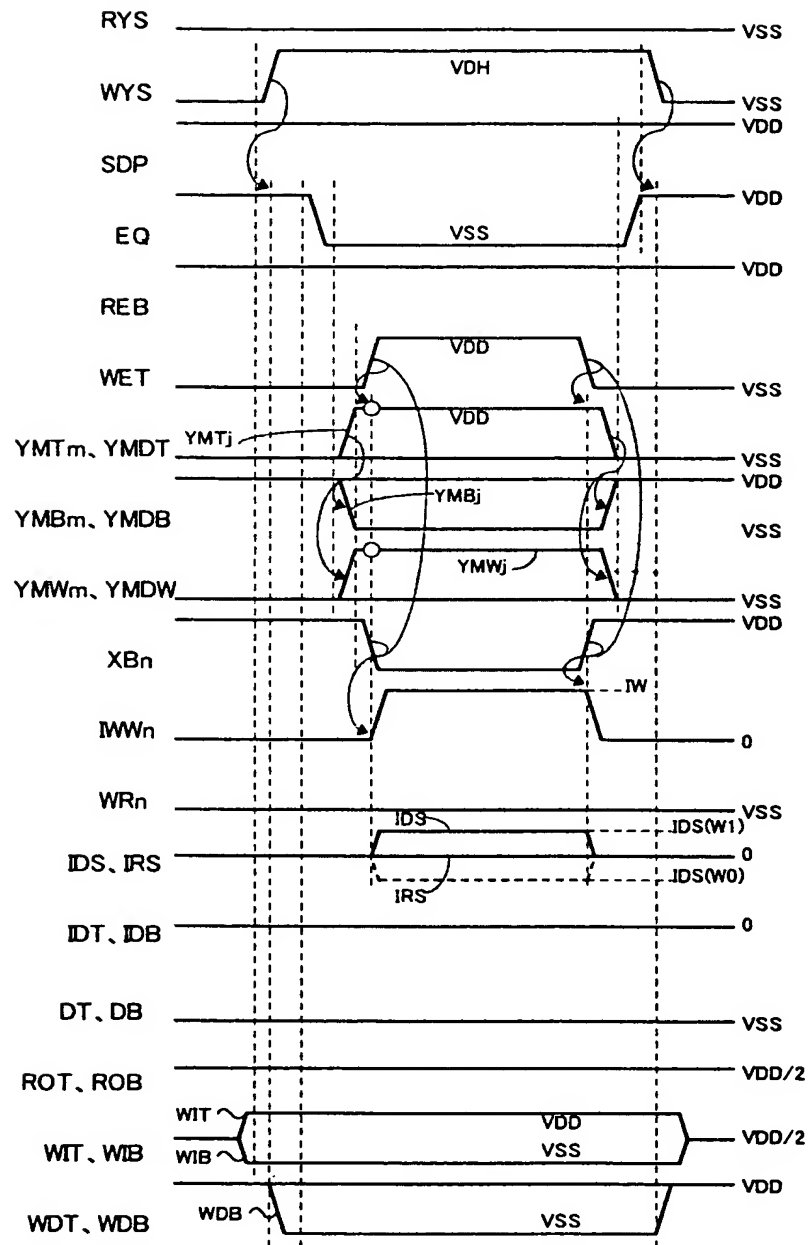


FIG. 10

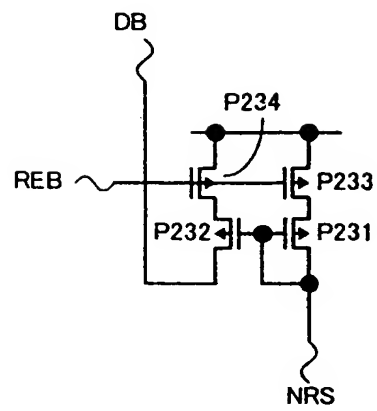


FIG. 11

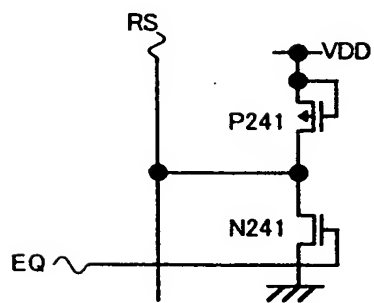


FIG. 12

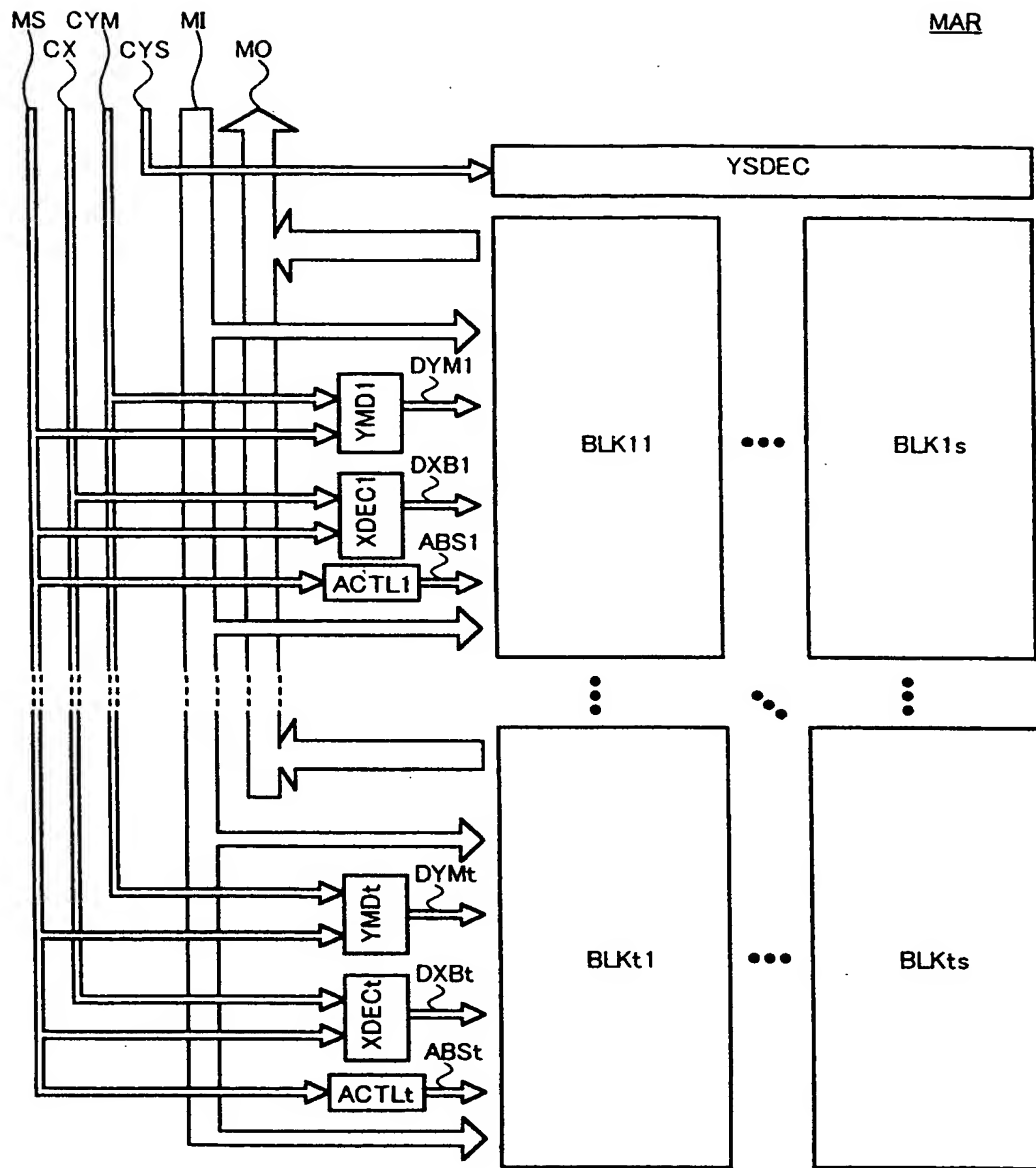


FIG. 13

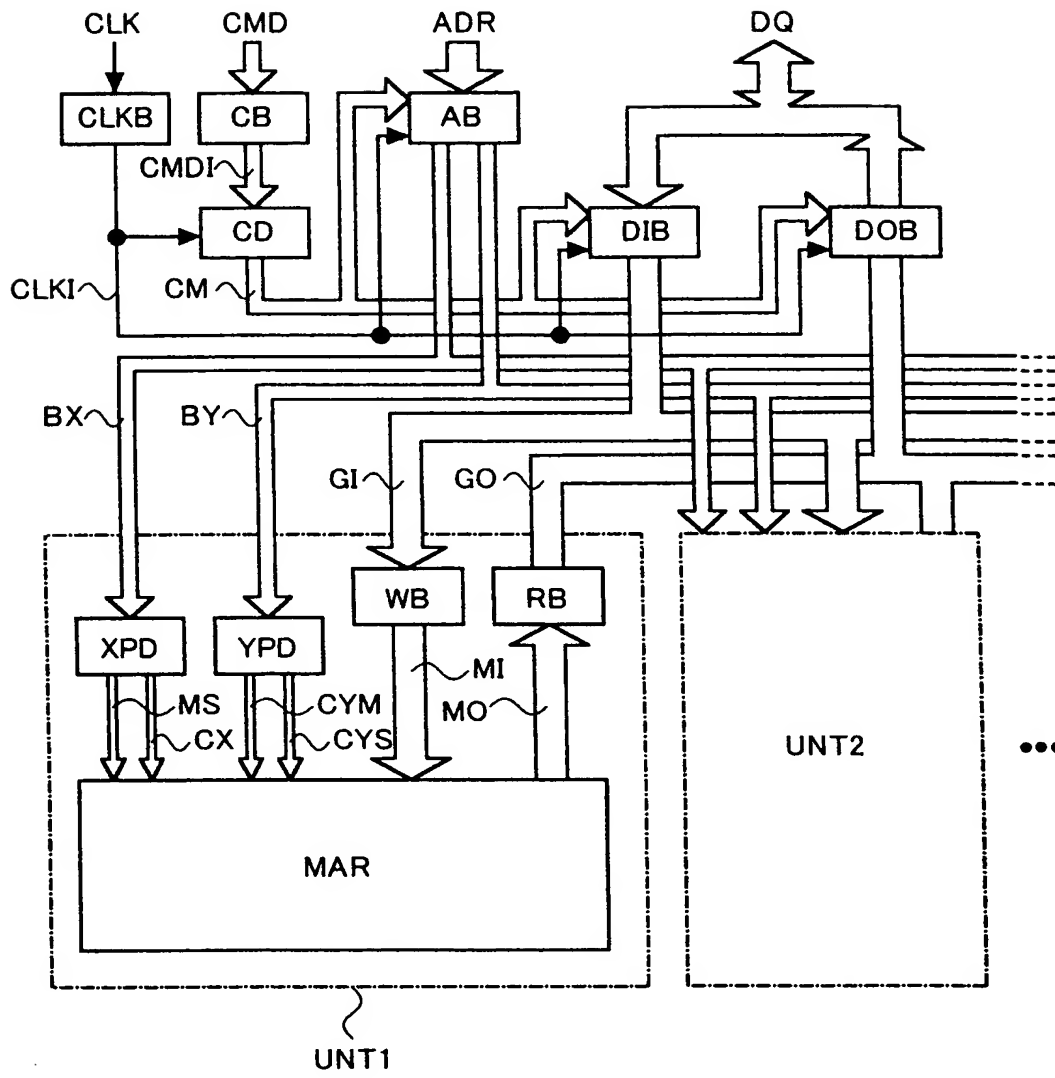


FIG. 14

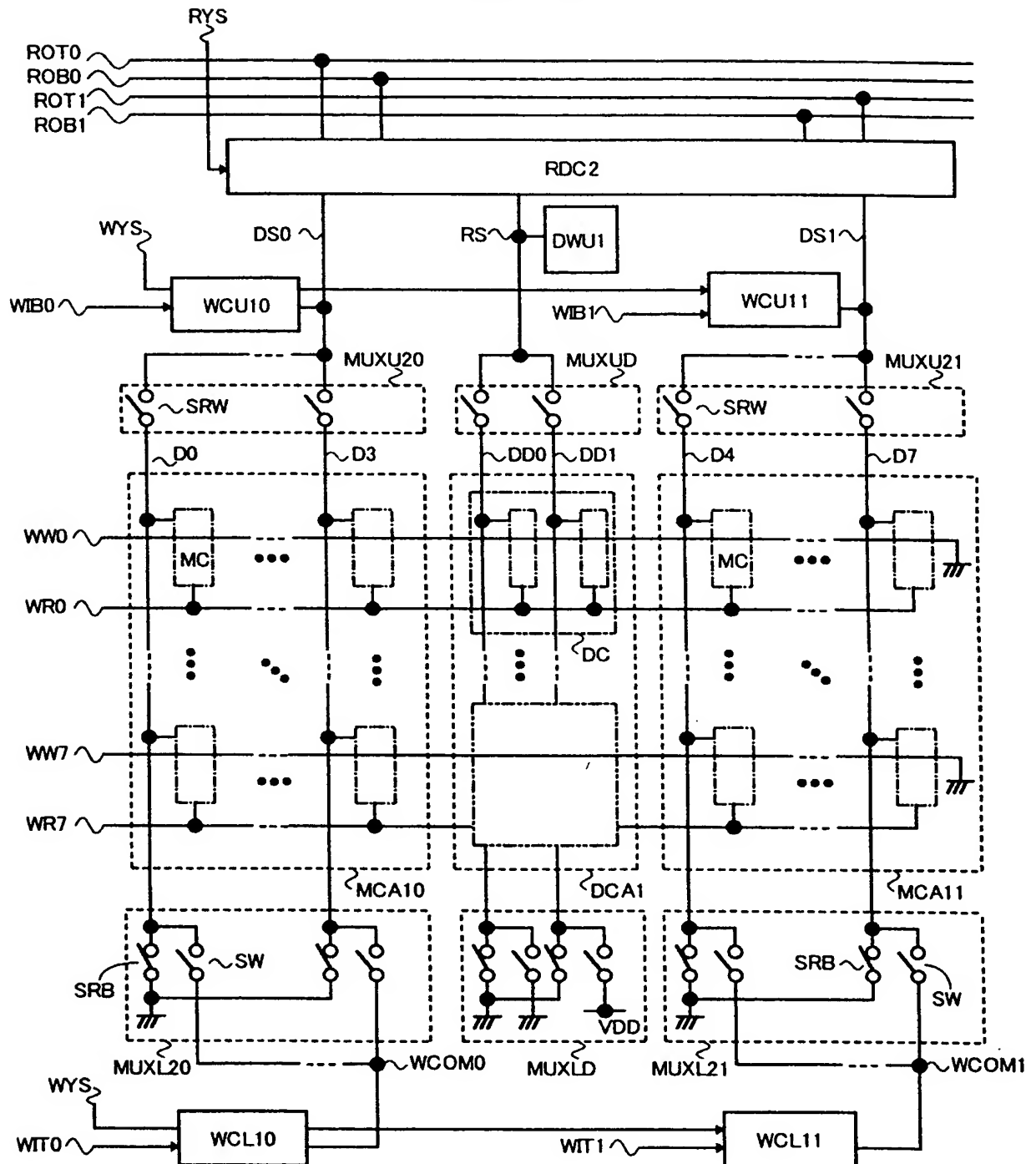


FIG. 15

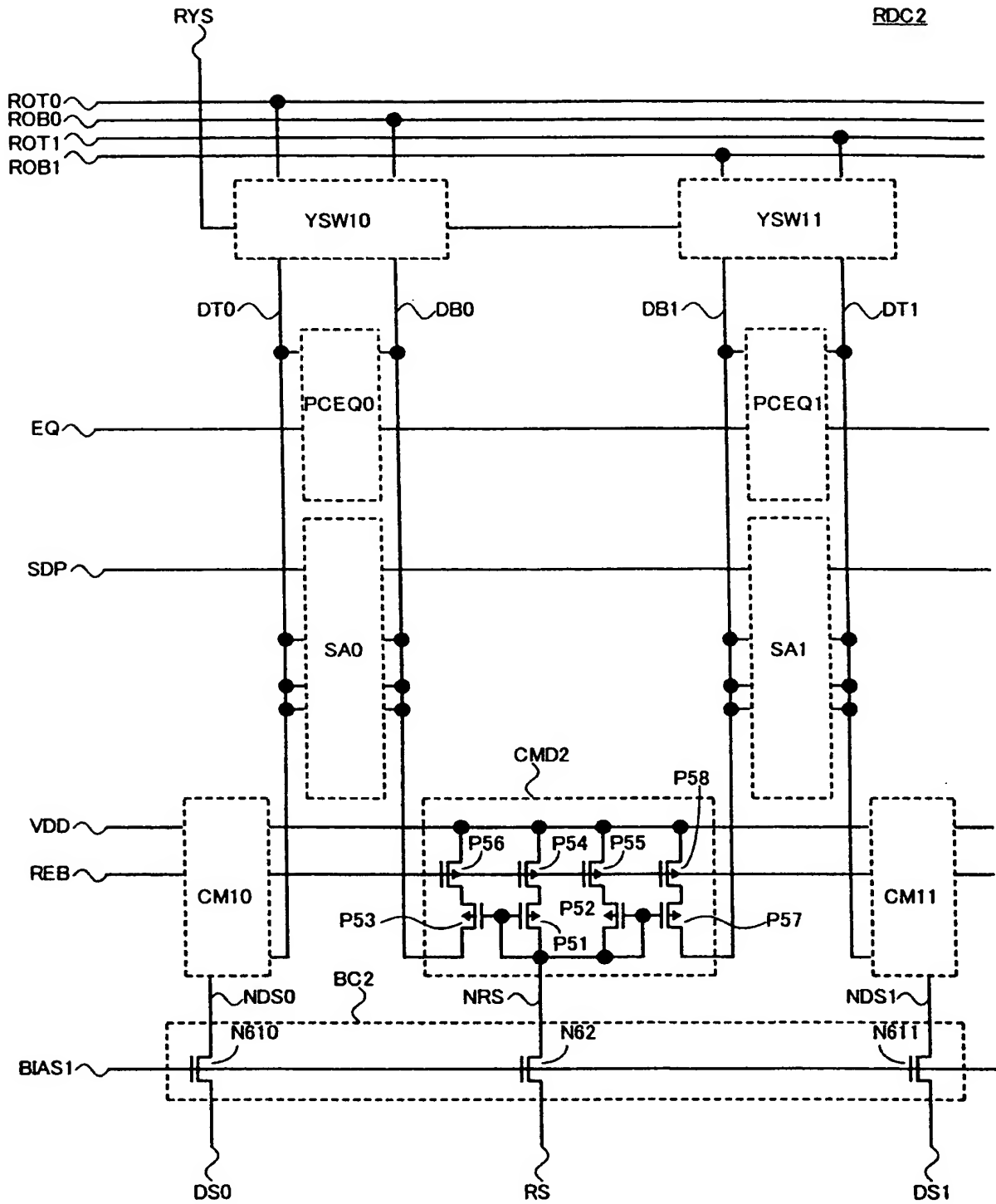


FIG. 16

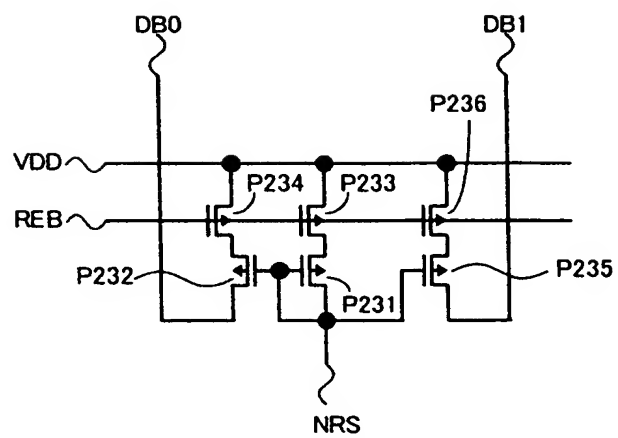


FIG. 17

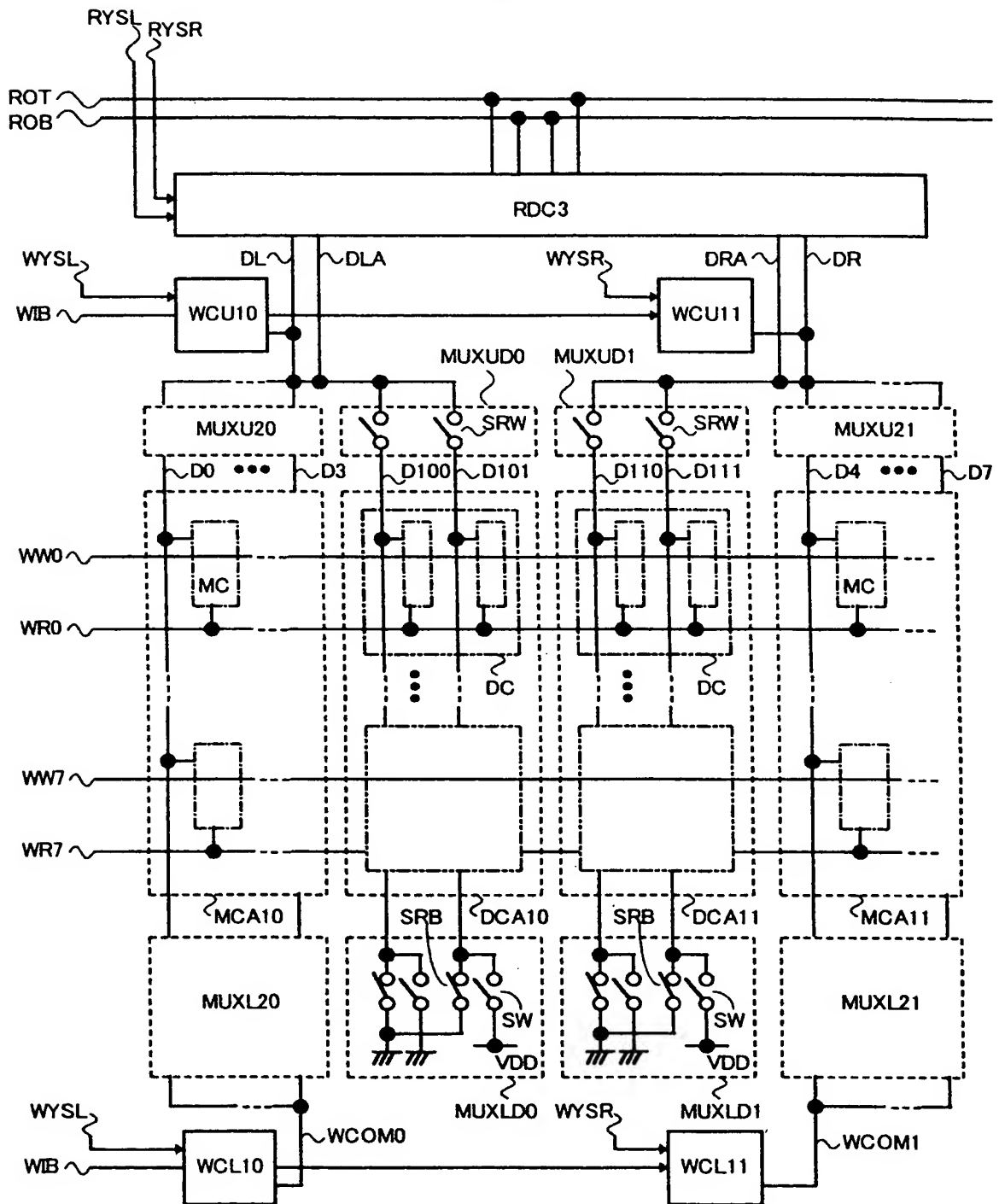


FIG. 18

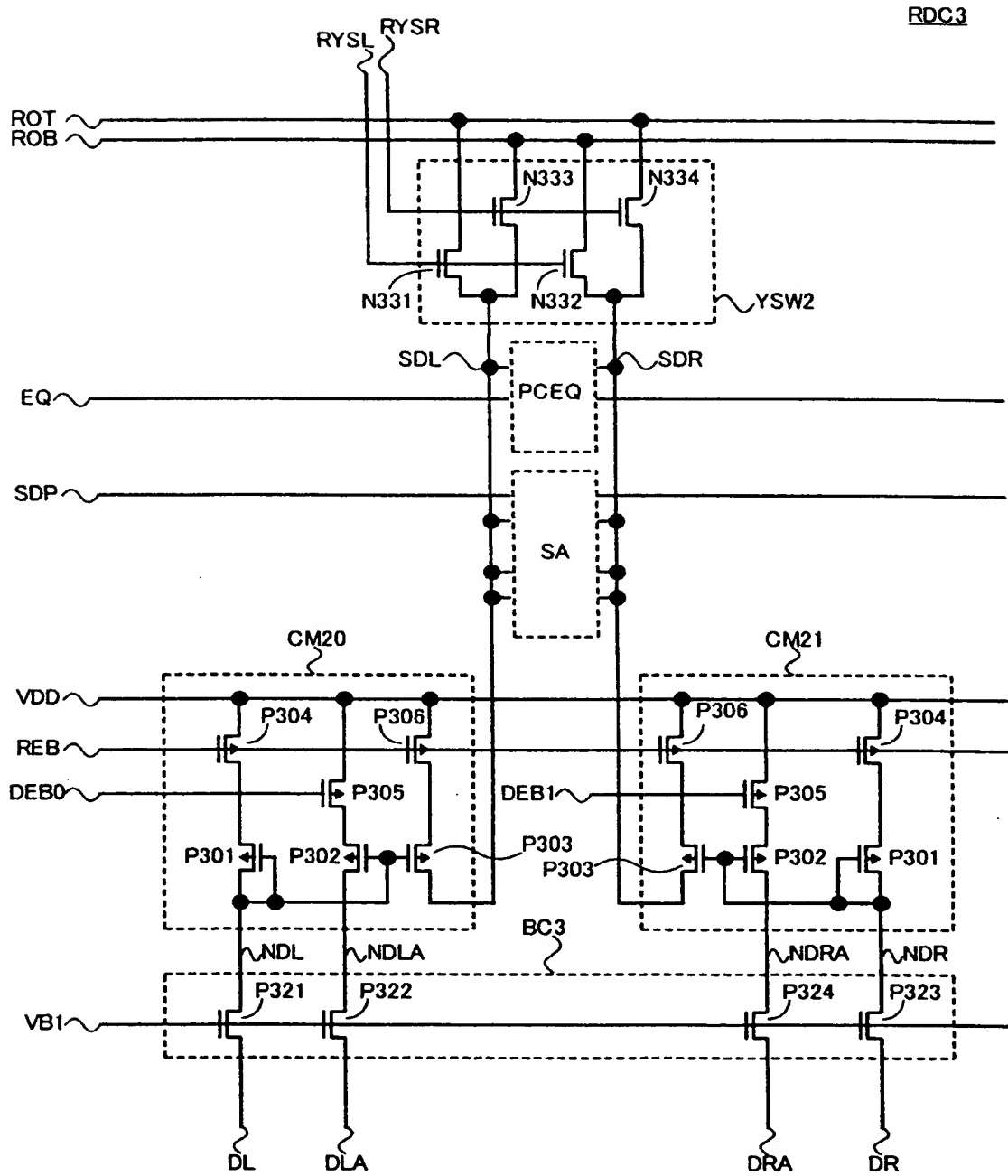


FIG. 19

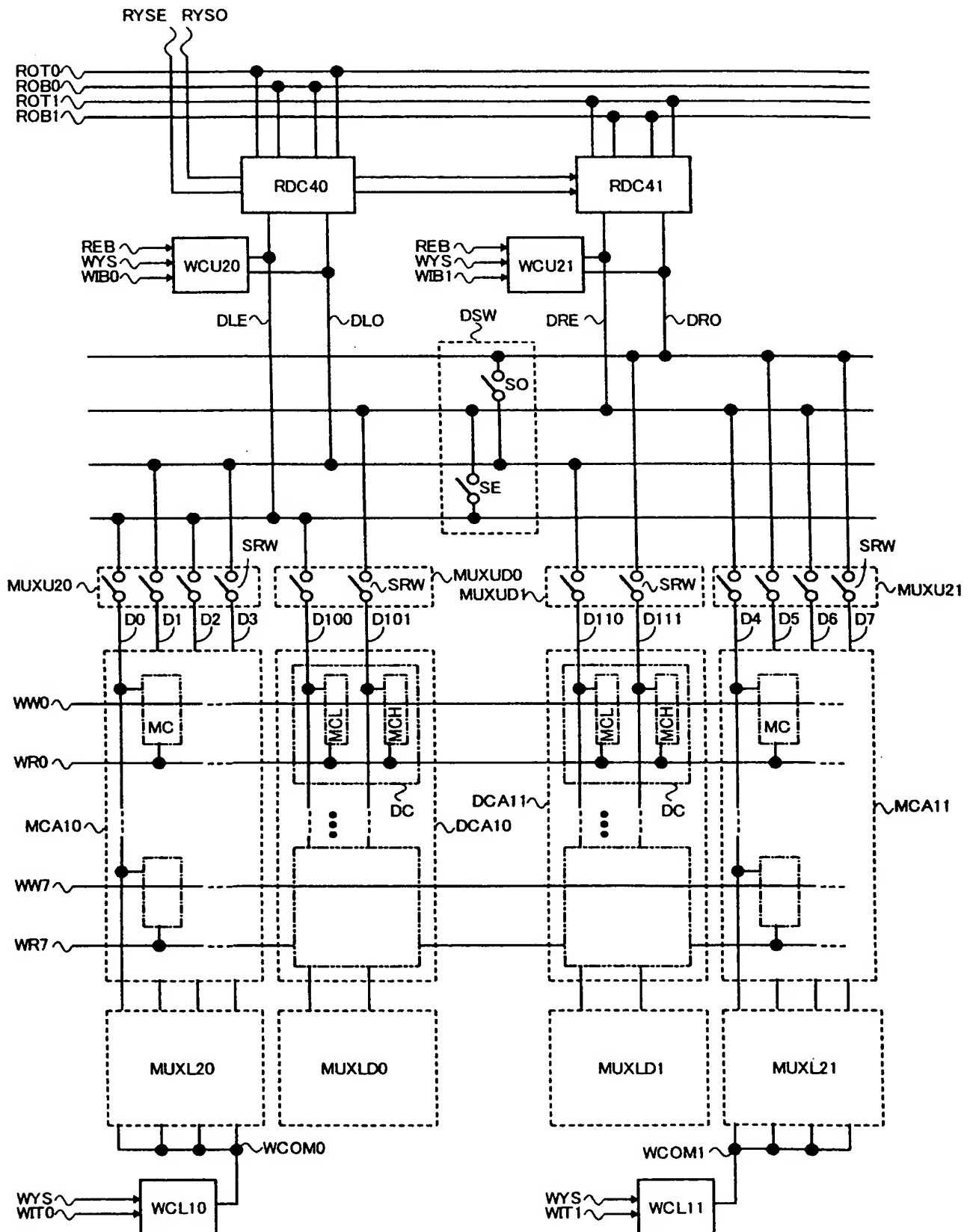


FIG. 20

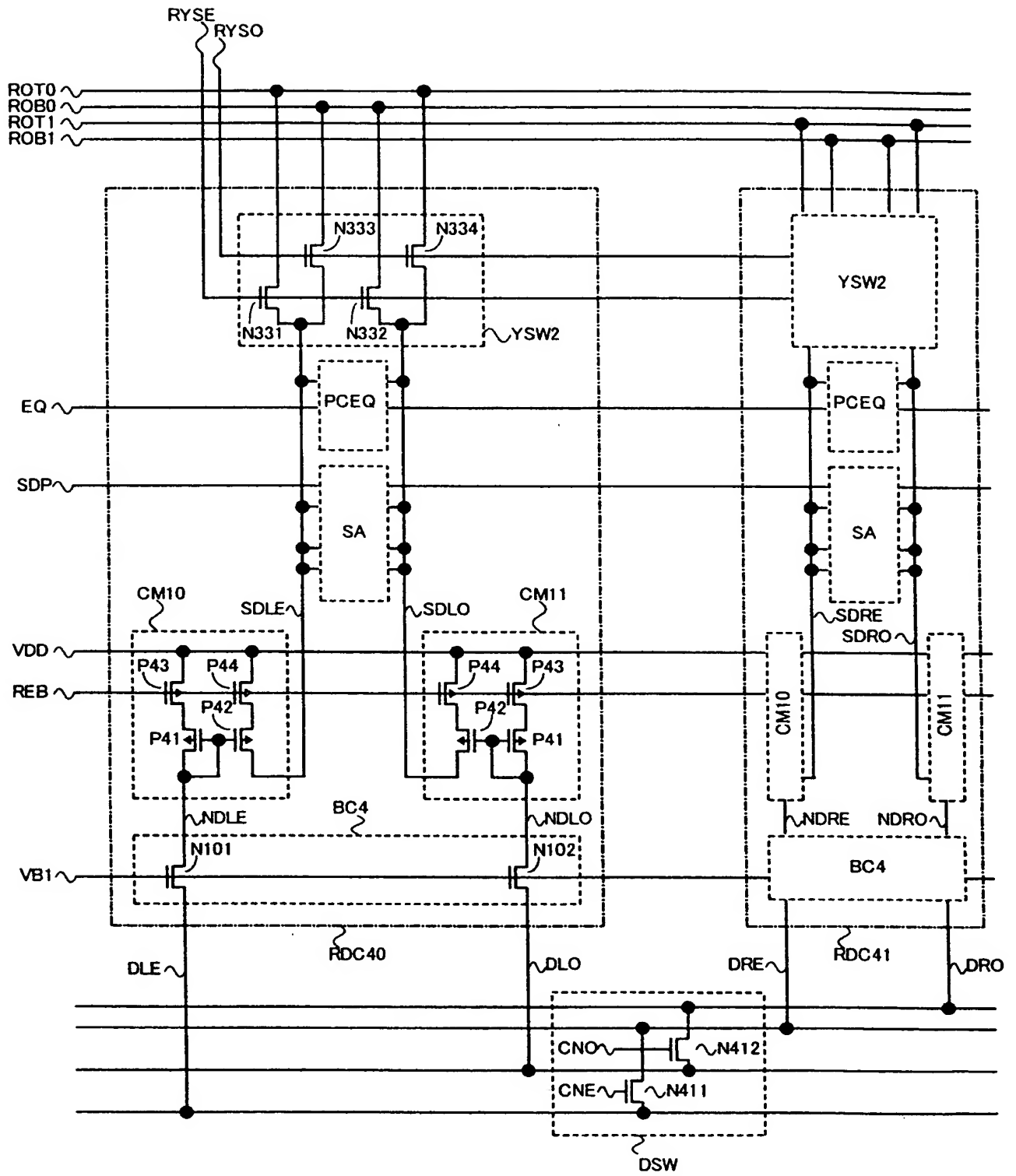


FIG. 21

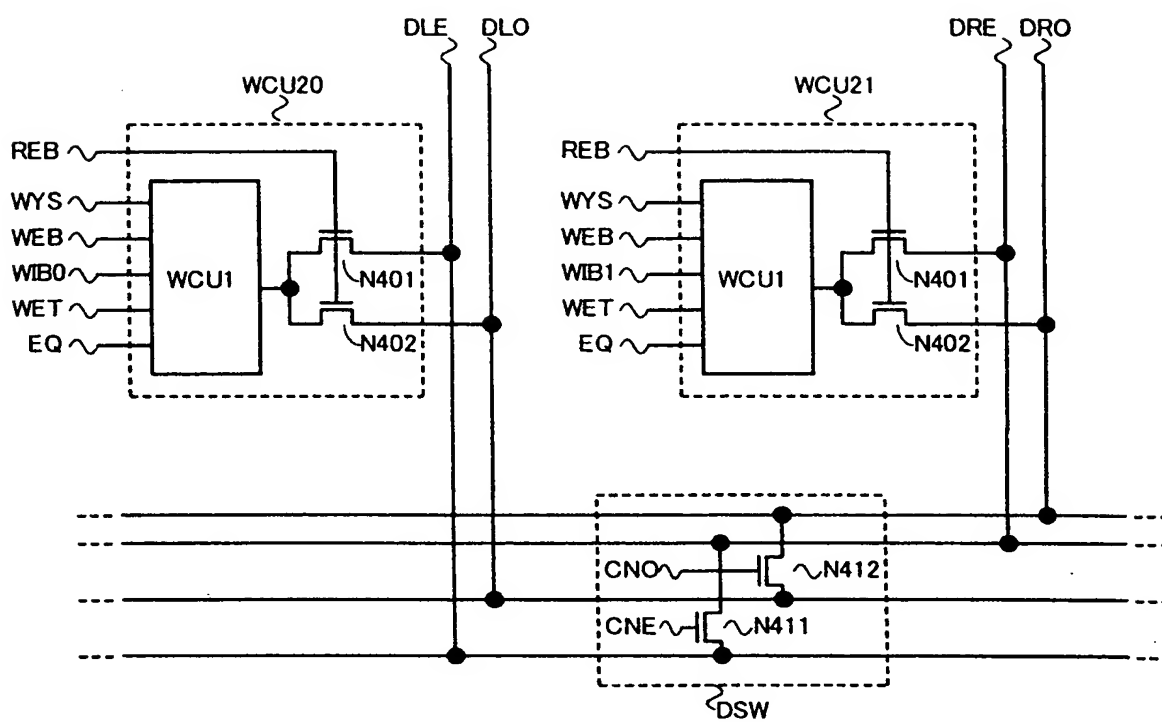


FIG. 22

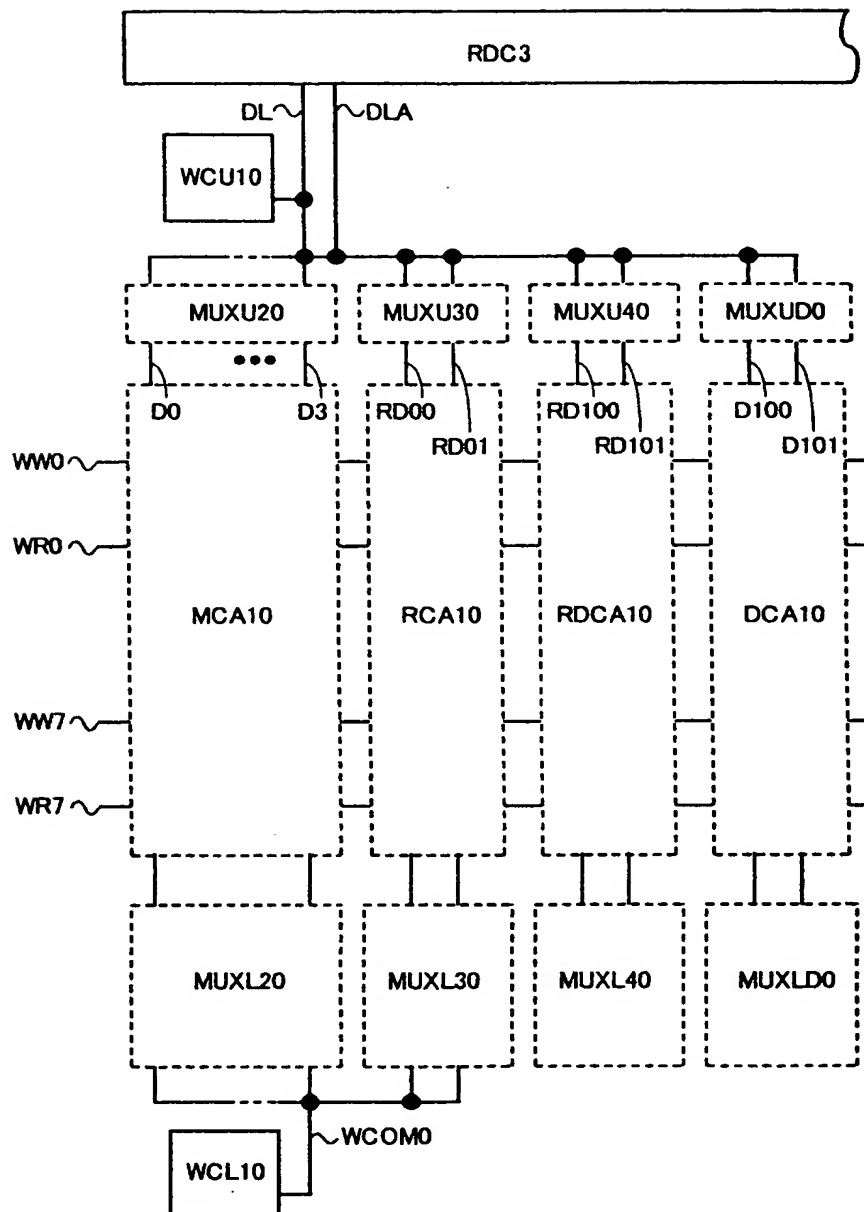


FIG. 23

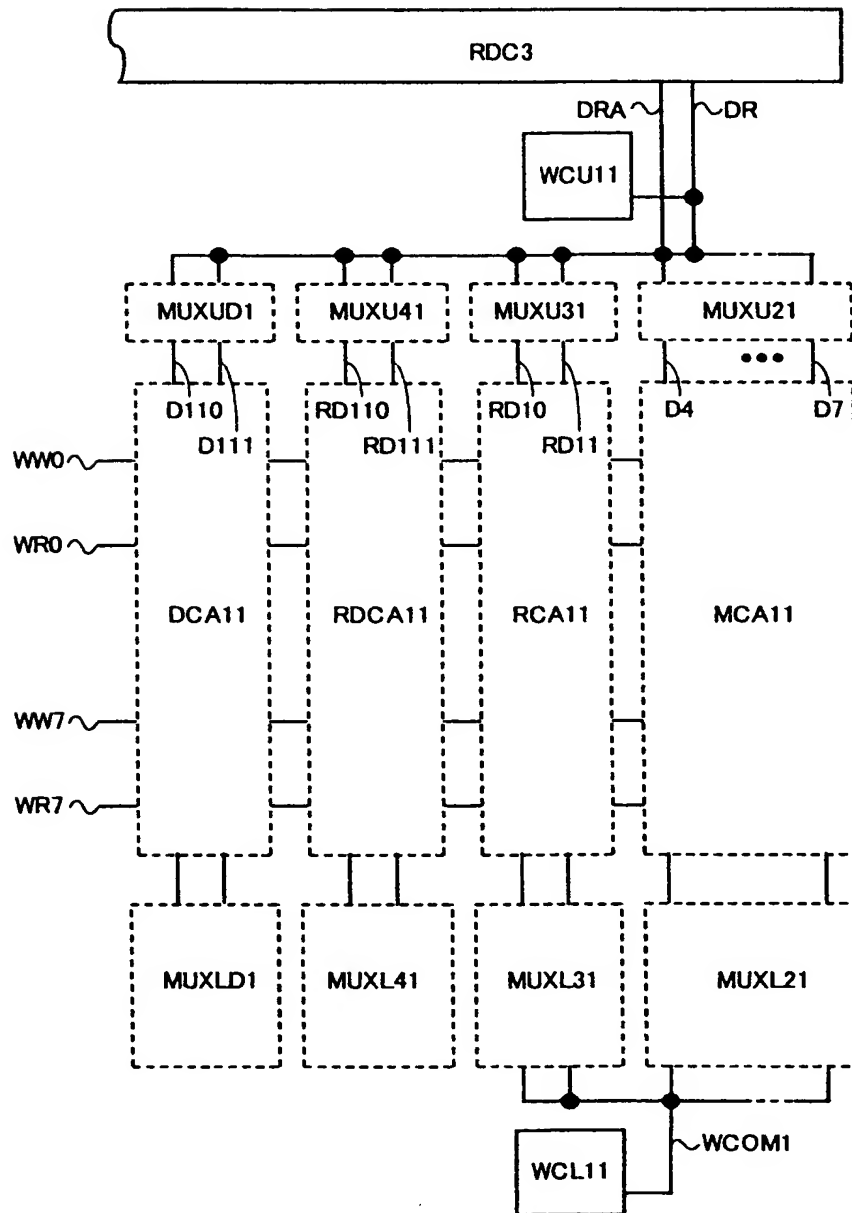


FIG. 24

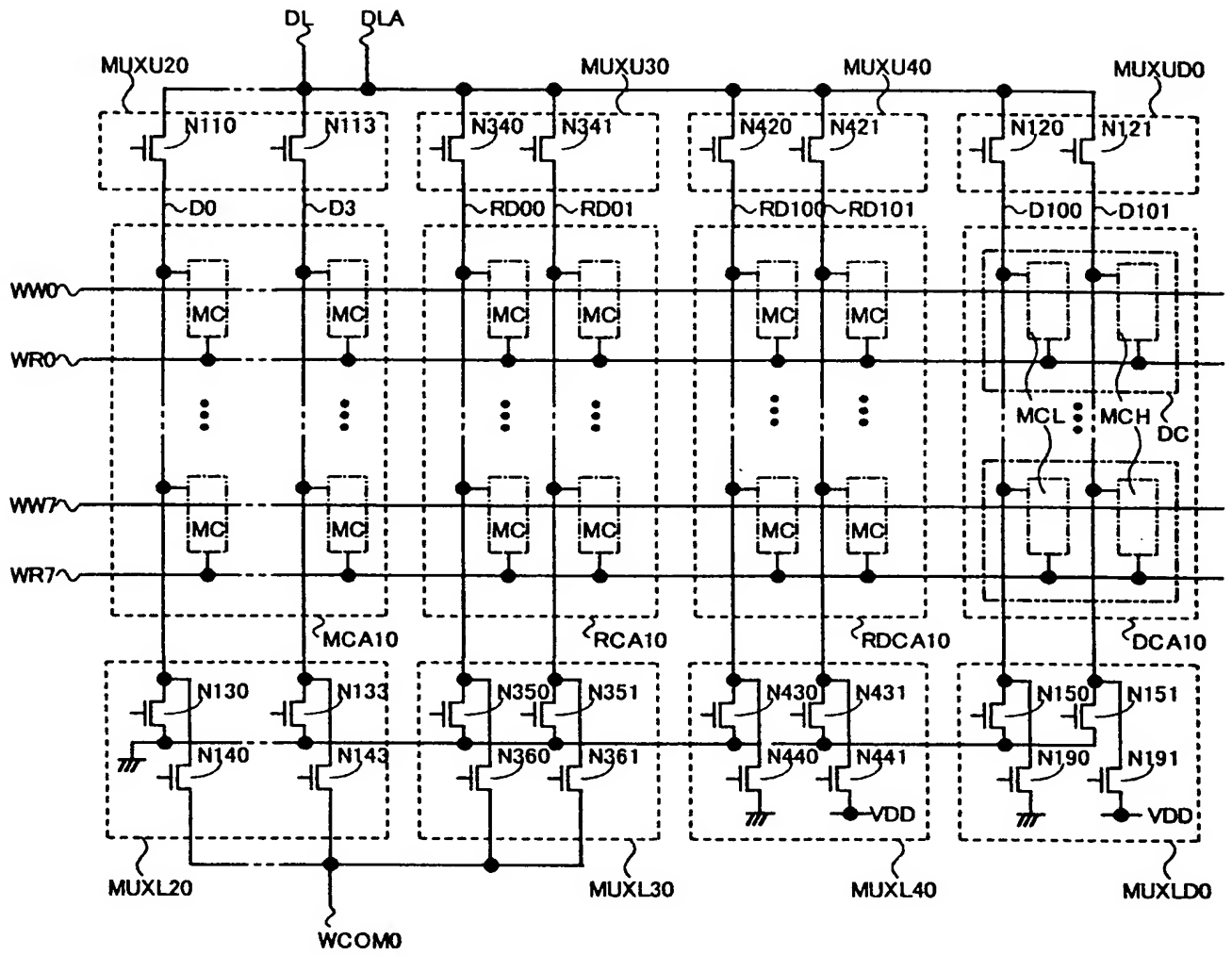


FIG. 25

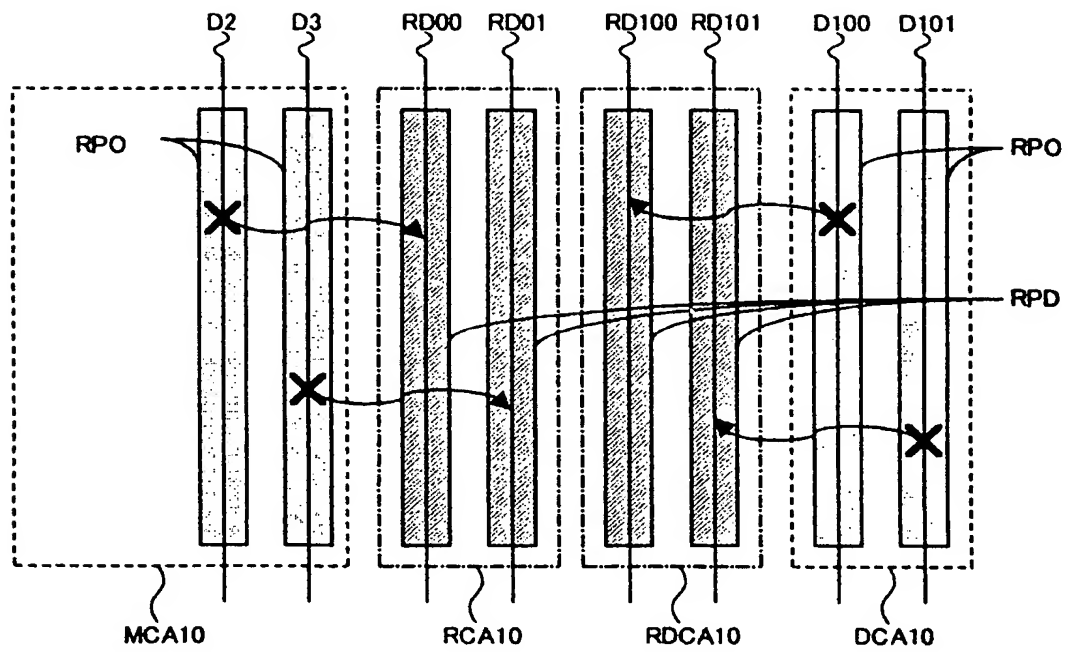


FIG. 26

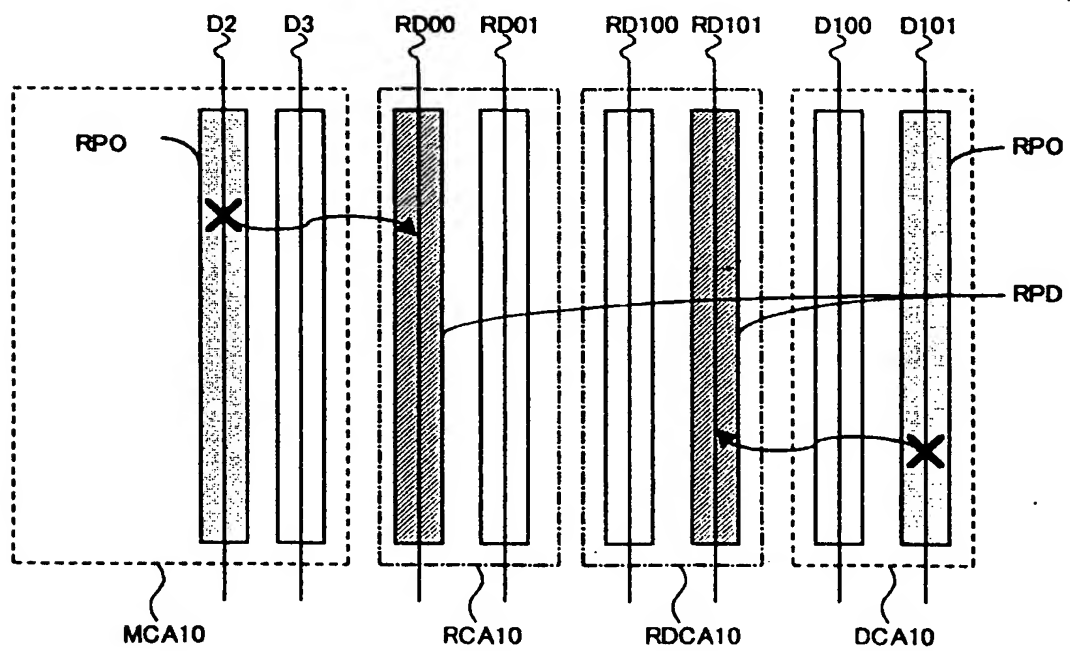


FIG. 27

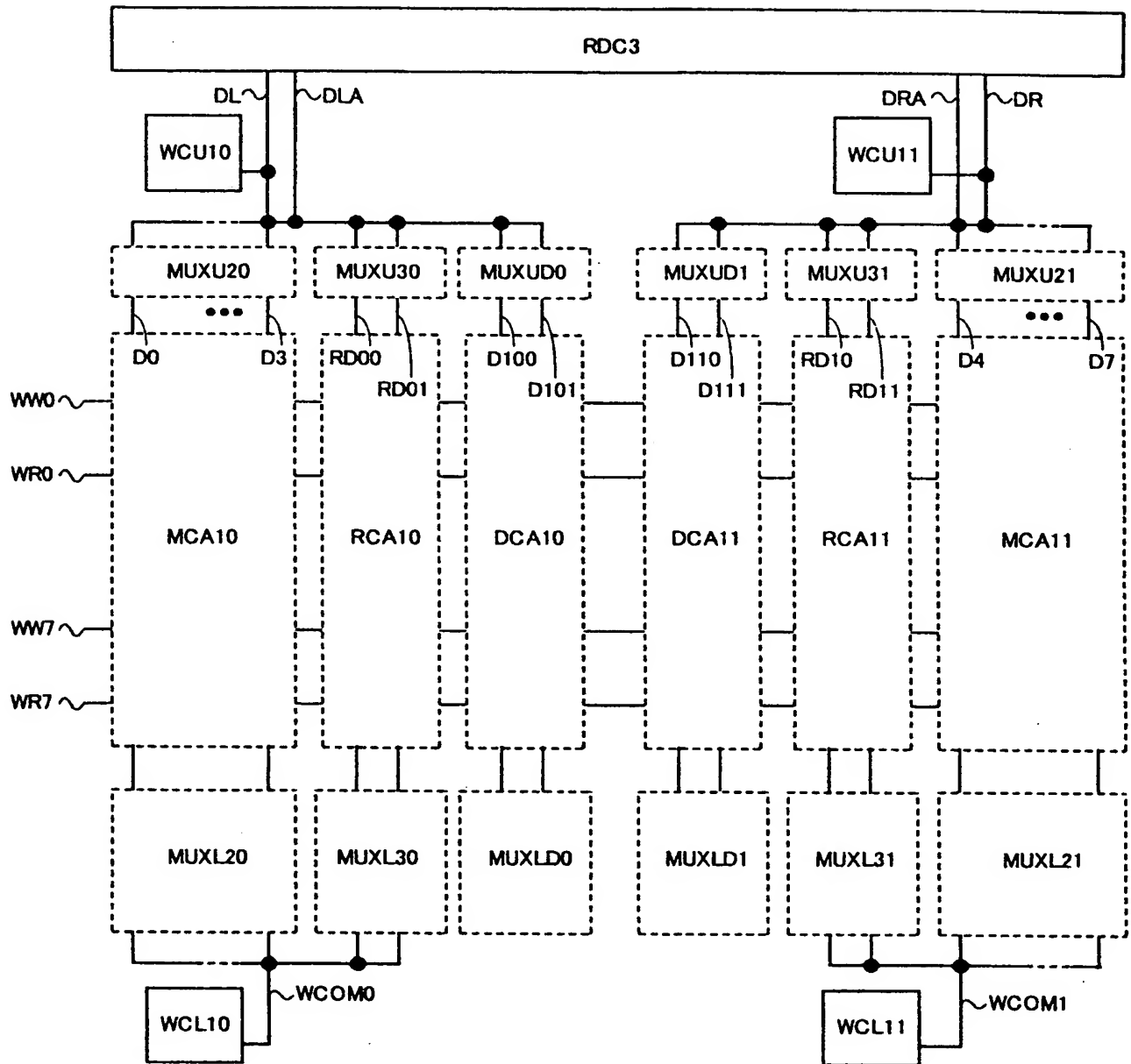


FIG. 28

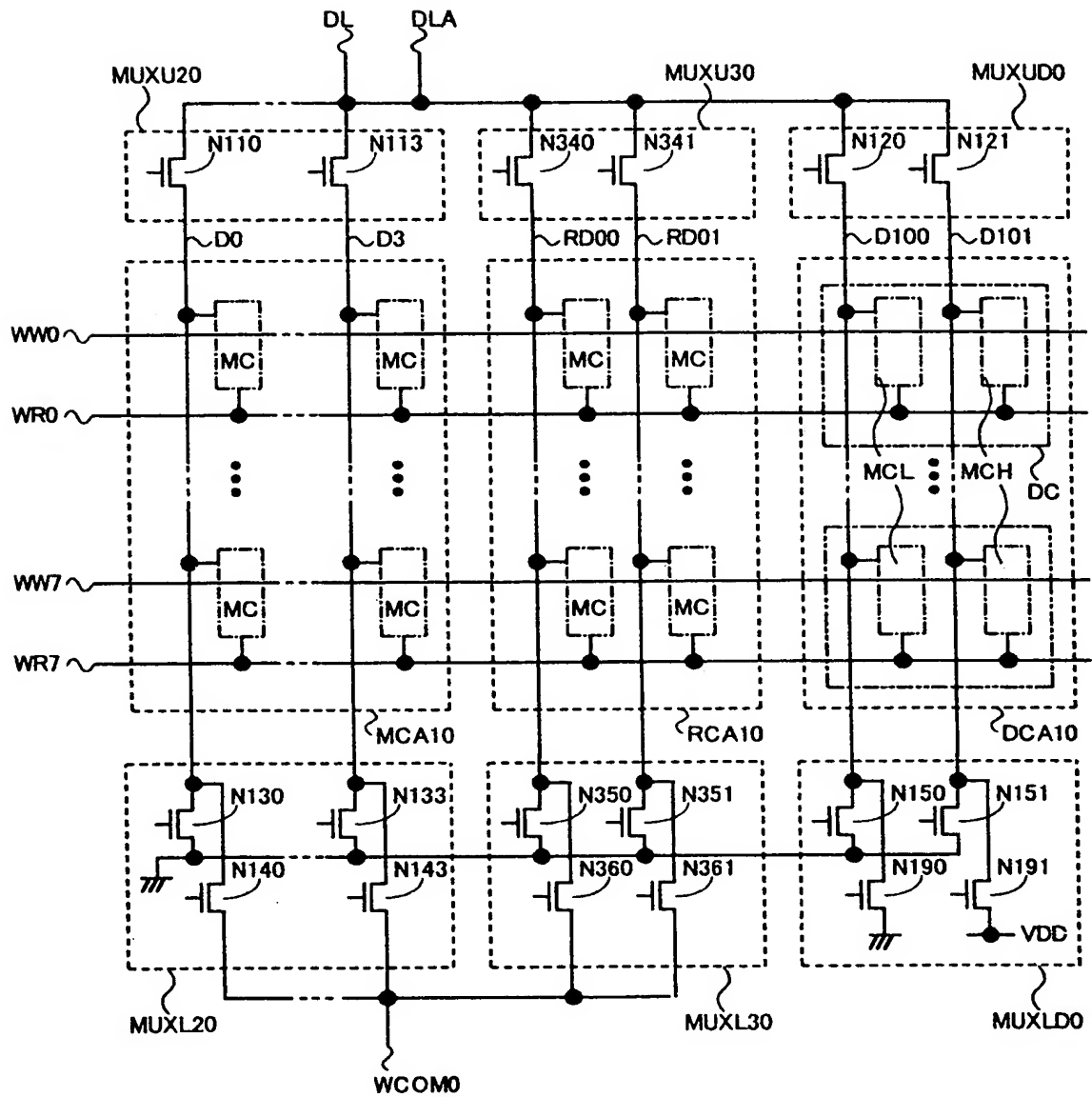


FIG. 29

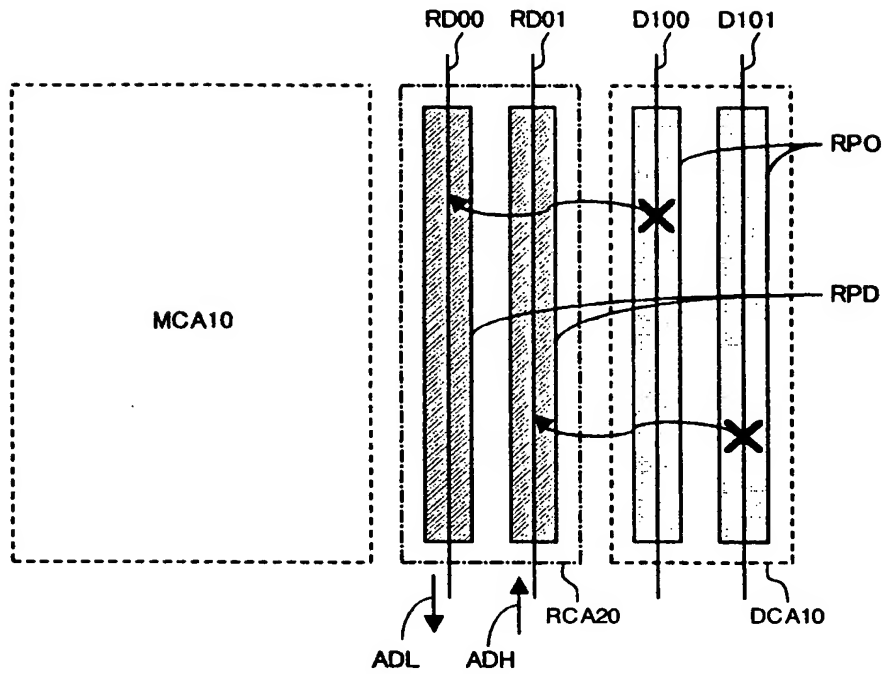


FIG. 30

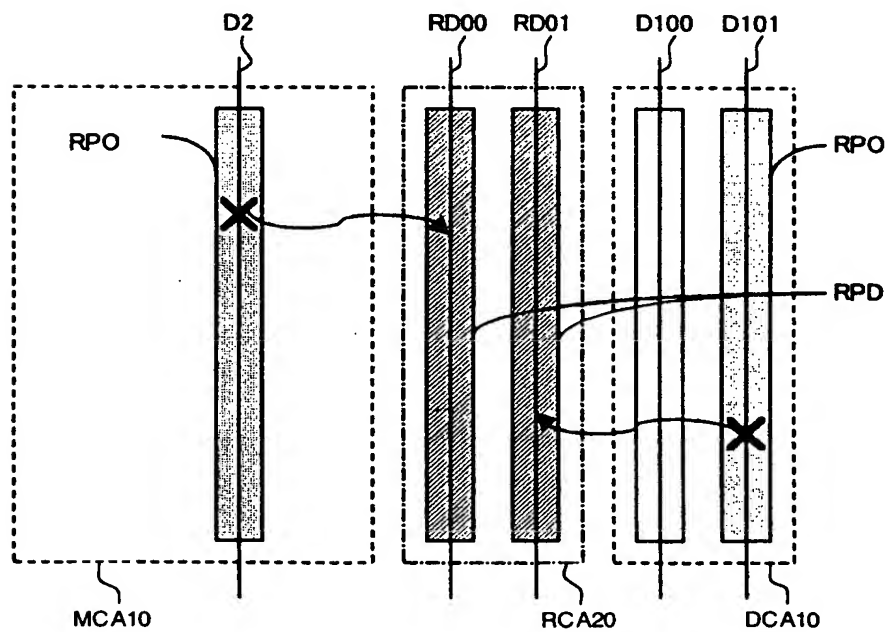


FIG. 31

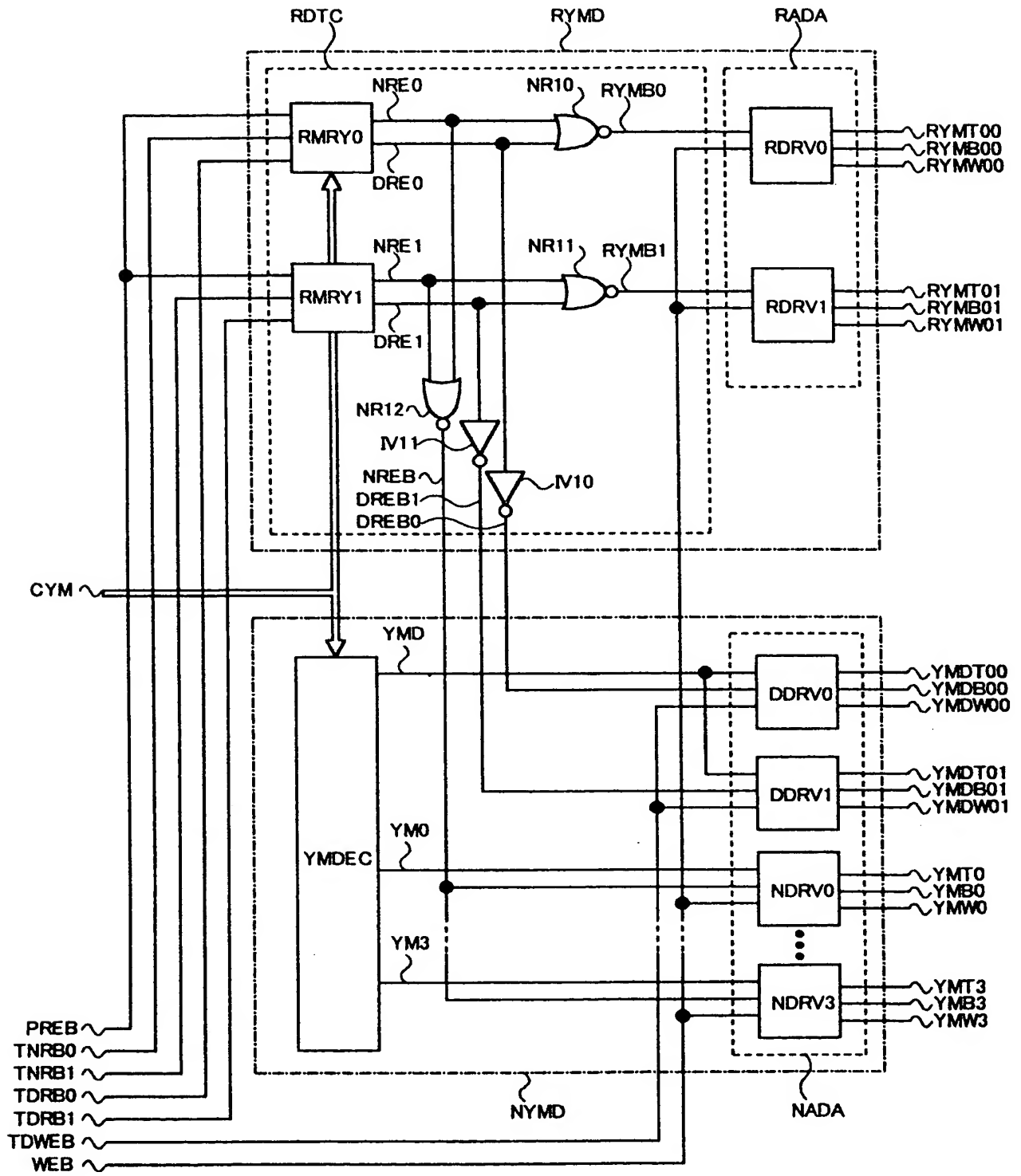


FIG. 32

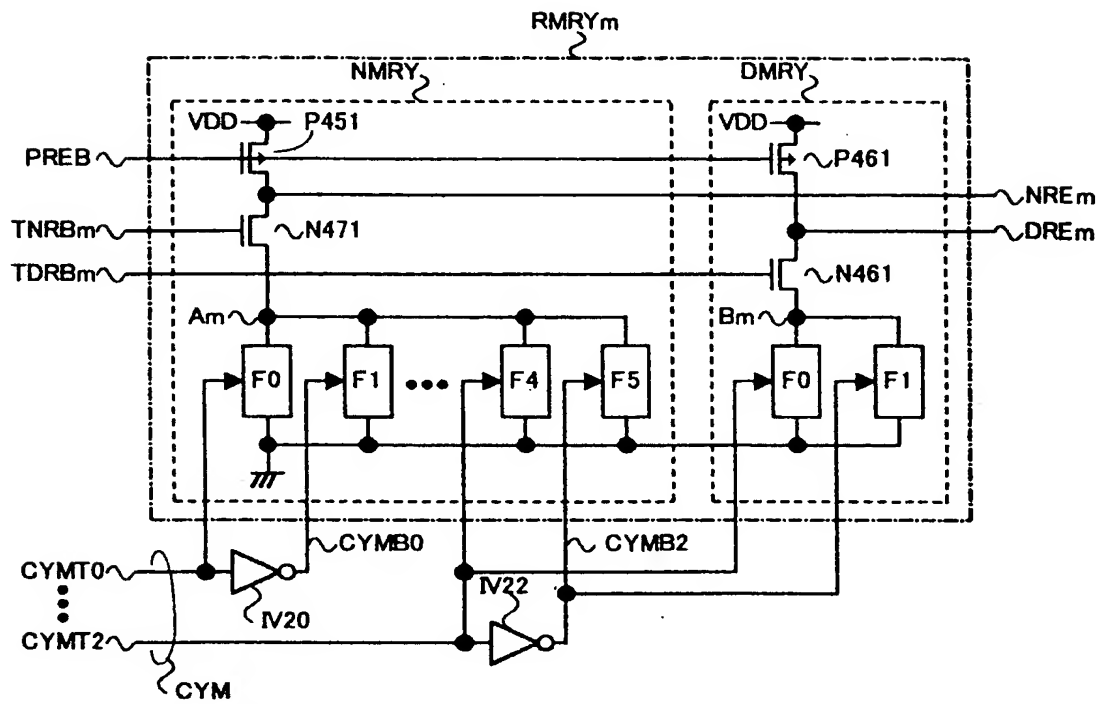


FIG. 33

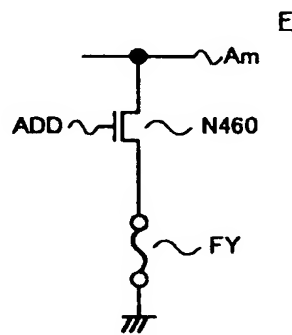


FIG. 34

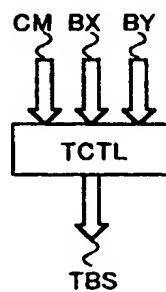


FIG. 35

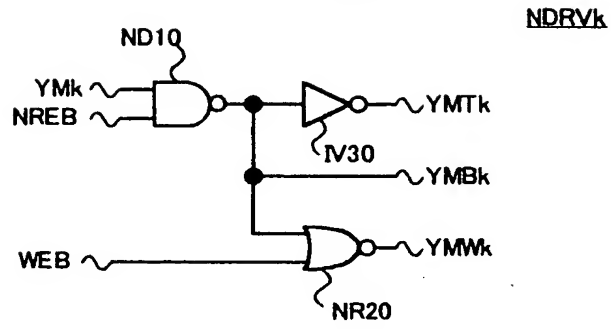


FIG. 36

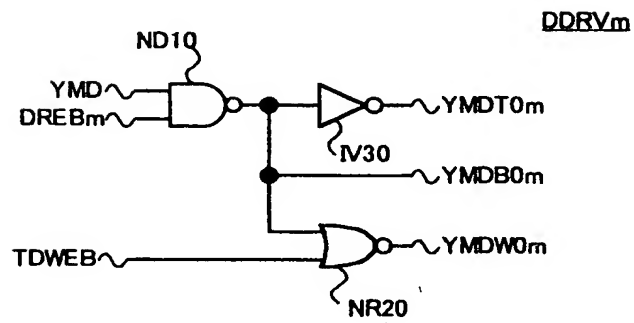


FIG. 37

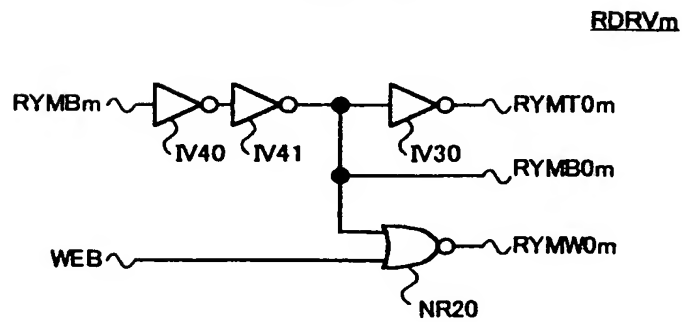


FIG. 38

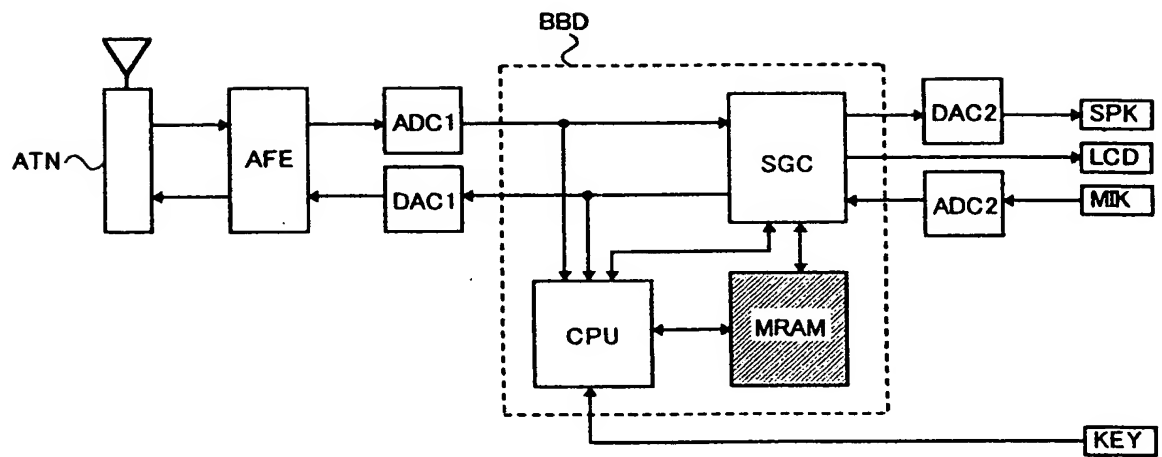


FIG. 39

MUX	NMOS	YMX	MUX	NMOS	RYMX
MUXU20	N110	YMT0	MUXU30	N340	RYMT00
	:	:		N341	RYMT01
	N113	YMT3	MUXL30	N350	RYMB00
MUXL20	N130	YMB0		N351	RYMB01
	:	:		N360	RYMW00
	N133	YMB3		N361	RYMW01
	N140	YMW0	MUXU40	N420	RYMDT00
	:	:		N421	RYMDT01
	N143	YMW3	MUXL40	N430	RYMDB00
MUXUD0	N120	YMDT00		N431	RYMDB01
	N121	YMDT01		N440	RYMDW00
MUXLD0	N150	YMDB00		N441	RYMDW01
	N151	YMDB01			
	N190	YMDW00			
	N191	YMDW01			